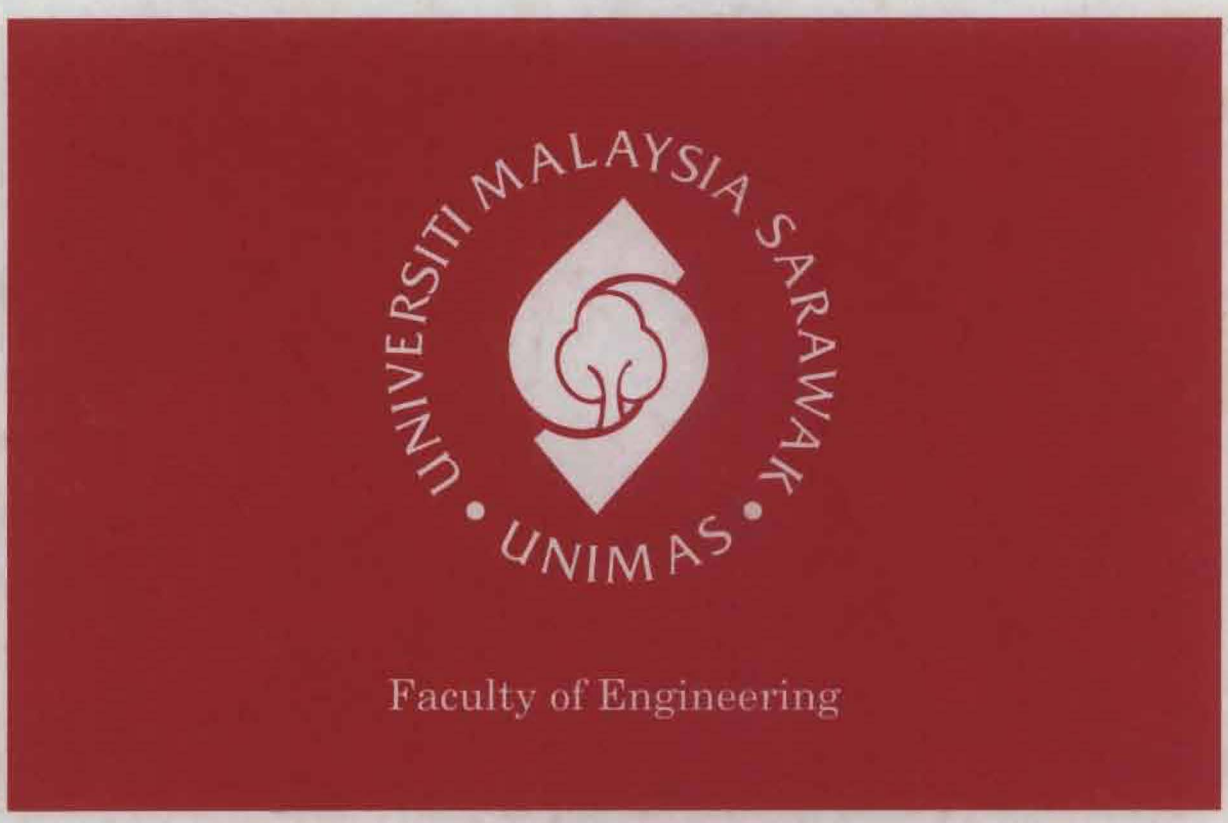

A HIGH SPEED TRISTATE BUFFER

Nurul Hidayah Binti Hairuddin

Bachelor of Engineering with Honours
(Electronics and Computer Engineering)
2006

A HIGH SPEED TRISTATE BUFFER

NURUL HIDAYAH BINTI HAIRUDDIN

This project is submitted in partial fulfillment of
the requirements for the degree of Bachelor of Engineering with Honors
(Electronics & Computer Engineering)

Faculty of Engineering
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Judul: **A HIGH SPEED TRISTATE BUFFER**

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telah dibaca dan disahkan oleh:

7 April 2006

Puan Rohana Bt Sapawi

Penyelia

Tarikh

Dedicated to my beloved parent, brothers, lecturers and friends.
I love you so much...

ACKNOWLEDGMENT

Bismillahirrahmanirrahhim…

"In the name of Allah most gracious and most merciful"

First and foremost, I would like to dedicate this project to my parent and family members for their supports, encouragements and loves during the period of study.

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ABSTRAK

Projek ini memaparkan rekaan litar penampan CMOS dengan kelajuan tinggi yang berkeupayaan untuk memacu kapasitan yang lebih besar berbanding litar penampan CMOS biasa. Teknik yang digunakan dalam merekacipta litar ini adalah berdasarkan litar *"feedback"* yang dapat mencapai ayunan penuh dari pembekal voltan ke pembumian. Dalam projek yang dijalankan ini juga dimasukkan keputusan hasil simulasi daripada litar yang dicadangkan berkenaan masa kelambatan, masa naik, masa turun dan juga arus asas semasa *"enable"* dengan menggunakan program Pspice. Selain berkelajuan lebih tinggi, penampan ini memberi sumbangan dalam penggunaan pembekal voltan yang optimum.

ABSTRACT

This project presents a high speed CMOS tristate buffer design circuit which has the capability to drive larger capacitive load compared to the conventional CMOS tristate buffer. The technique used is based on the feedback circuit to achieve a full swing operation from supply voltage to ground. In this project also included the simulative results of propagation delay, rise time, fall time and base current during enable by using Pspice. Besides having higher speed, the proposed tristate buffer contributed in optimum power supply consumption.

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LIST OF ABBREVIATION

C	Capacitance
C_L	Capacitive load
CMOS	Complementary Metal-Oxide Semiconductor
EDP	Energy delay product
f_{max}	Maximum frequency
GND	Ground
IC	Integrated Circuit
I_{peak}	Peak current
J	joules
PUN	Pull-up network
PDN	Pull-down network
PDP	Power delay product
P_{av}	Average power
R_{onN}	On resistance for NMOS transistor
R_{onP}	On resistance for PMOS transistor
t	Time
t_f	Fall time
t_P	Average propagation delay
t_{PHL}	High to low propagation delay
t_{PLH}	Low to high propagation delay
t_r	Rise time
V_{BS}	Source bulk voltage for NMOS transistor
V_{DD}	Drain to drain voltage

V_H	Voltage High
V_{in}	Input voltage
VLSI	Very Large Scale Integrated
V_o	Output voltage
V_{SB}	Source bulk voltage for PMOS transistor
V_{SG}	Source to gate voltage
V_{SS}	Source to source voltage
V_T	Threshold voltage
V_{T0}	Threshold voltage at zero bias
V_{TN}	Threshold voltage for NMOS
V_{TP}	Threshold voltage for NMOS
W/L	Width / length
Z	High impedance

CHAPTER 1

INTRODUCTION

1.1 Introduction

The massively used of tristate buffer in digital Very Large Scale Integrated (VLSI) systems including microprocessor and memory has required it to work in higher speed. This is the consequence of the thirst of technology for its rapid growth.

For this reason, a tristate buffer of Complementary Metal-Oxide Semiconductor (CMOS) technology will be designed for a higher speed. It is an important part inside the circuit which will cause to the whole digital system operation to work in a better condition or not due to its appearance. Most of the electronic circuits especially in the computers required this tristate buffer since it is connected to the bus. When other device is sending on the bus, all other sending devices should be disconnected. This can be achieved by setting the output buffers of those devices in high impedance state that effective disconnect the gate from output wire [1]. This is an advantage of tristate buffer over a normal buffer for its enable input to control the incoming signals.

In this project, a high speed performance of tristate buffer will be designed using PSpice tool. For the requirement of tomorrow's technology, this tristate buffer will also be designed to drive higher capacitive loads.

1.2 Principle Objectives

In order to gain a good result, every project should have specific objectives which must be achieved at the end of the project. This is one way of encouragement for a better work out. The objectives of this project are:

i. To design a high speed tristate buffer based on CMOS technology.
ii. To design tristate buffer that can drive larger capacitive load which is suitable for driving a data bus.
iii. To develop and simulate circuits using PSpice.

1.3 Chapter Overview

The report documentation of this project is organized into five chapters. The first chapter generally introduces the tristate buffer. It also explains in brief the objectives and overview of the project.

Chapter 2 will present a brief discussion due to the performance and behavior of the CMOS circuit. The characteristics and parameters of the

device will also be discussed in this chapter. This information will guide to design and contribute to a better performance circuit than the current design.

In Chapter 3 will explain the methodology to design the proposed CMOS tristate buffer with the technique which has been used. The description of the conventional design is explained in this chapter so the comparison of the circuits can be observed.

The simulation derived from the design in Chapter 3 will be discussed in Chapter 4. The discussion is about the development of the program simulation using simulation tool and also based on the results and observations.

Chapter 5 will conclude the overall project which has been done throughout two semesters. Recommendations for better work in the future will be suggested due to discussions from the previous chapter.

CHAPTER 2

LITERATURE REVIEW

2.1 Complementary Metal-Oxide-Semiconductor (CMOS)

CMOS technology is by a large margin the most dominant of all the IC technologies available for digital-circuit design. CMOS has replaced NMOS, which was employed in the early days of VLSI in the 1970s. There are a number of reasons for this development, the most important of which is the much lower power dissipation of CMOS circuits. CMOS has also replaced bipolar as the technology of choice in digital-system design and has made possible levels of integration (or circuit packing densities) and a range of applications that would never have been possible with bipolar technology. Furthermore, CMOS continues to advance, whereas there appear to be few innovations at the present time in bipolar digital circuits [2].

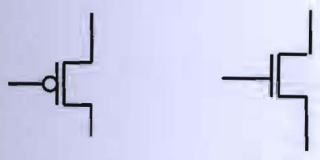
Some of the reasons for CMOS displacing bipolar technology in digital applications are because CMOS logic circuits dissipate much less power than bipolar logic circuits and thus one can pack more CMOS circuits on a chip than is possible with bipolar circuits [2].

The feature size (that is minimum channel length) of the MOS transistor has decreased dramatically over the years. This permits very tight circuit packing and correspondingly very high levels of integration [2].

All of these advantages had created an idea to build a tristate buffer using the CMOS. The next section will review the objectives of designing the tristate buffer and the overview after choosing the type of CMOS devices.

2.2 CMOS Inverter

In designing the tristate buffer, the CMOS device is chose as mentioned earlier in the previous chapter. But before the circuit is designed, the characteristics of the device should be investigated in order to build a good or even better circuit. In this chapter, the characteristics and performance of CMOS which related to tristate buffer will be covered. Before proceed with other explanation, the symbols of transistor used is acknowledged in Figure 2.1.



(a) PMOS (b) NMOS

Figure 2.1: Transistor symbols

Inverter is the basic device of constructing CMOS gate, including the tristate buffer. Figure 2.2 shows the static CMOS inverter. The source of the PMOS transistor is connected to V_{DD}, the source of the NMOS transistor is connected to V_{SS} (0 V), and the drain terminals of the two MOSFETs are connected together to form the output node. The substrates of both NMOS and PMOS transistors are connected to their respective sources, and so body effect is eliminated in both devices [3], where $V_{SB} = 0 = V_{BS}$ [4].

Simplified models for the CMOS inverter operation appear in Figure 2.2(a) and Figure 2.2(b). The input signal controls the state of the two switches that effectively work as a single-pole double throw switch. In Figure 2.2(b), the input is at a low input level ($V_{in} = 0$), and the output is connected to V_{DD} through the on-resistance of the PMOS transistor. In Figure 2.2(c), the input is at high input level ($V_{in} = V_{DD}$), and the output is connected to ground through the on-resistance of the NMOS transistor.

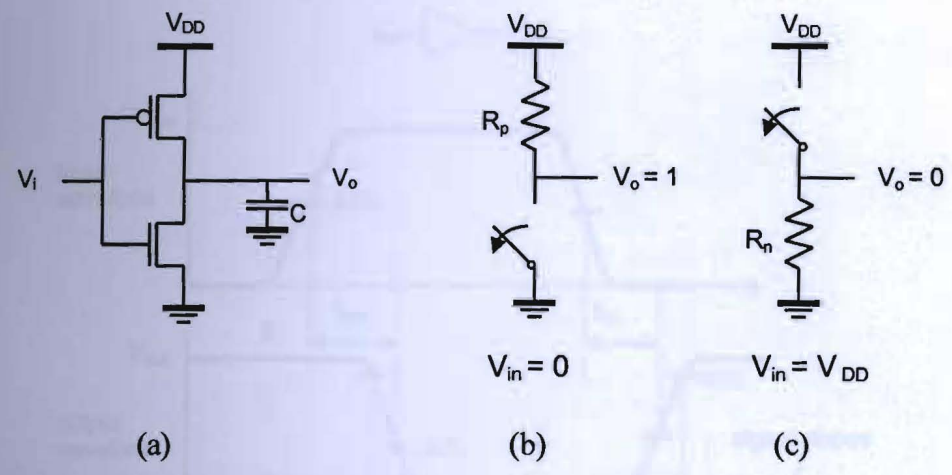


Figure 2.2: (a) CMOS inverter uses one NMOS and one PMOS transistor. (b) A simplified model of the inverter for a high input level. The output is forced to zero through the on-resistance of the NMOS transistor. (c) Simplified model of the inverter for a low input level. The output is pulled to V_{DD} through the on-resistance of the PMOS transistor [3].

2.2.1 Propagation Delay

Delay is one of the most important properties of a logic area. The majority of the chip designs are limited more by speed than by area. In this case, delays are estimated to gain high speed tristate buffer design. Delay is considered as the time it takes for a gate output to arrive at 50% of its final value as be shown in Figure 2.3 below.

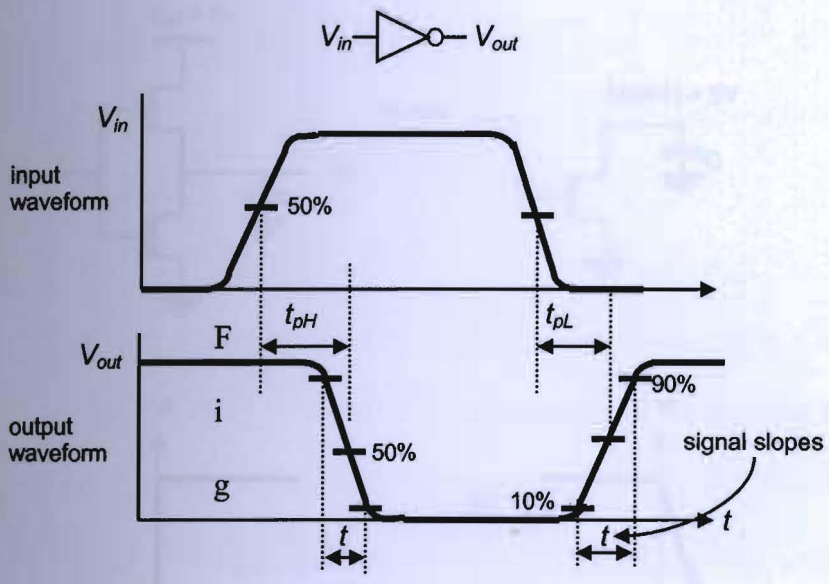


Figure 2.3: Propagation delay [4]

Propagation delay is caused by output capacitance; the input rise time, t_r and fall time, t_f, series of transistors, the supply voltage which higher V_{DD} causes delay, and temperature (the higher temperature causes more delay).

2.2.2 Transition, Rise and Fall Time of CMOS Inverter

Figure 2.4 illustrates the high-to-low output transition in a CMOS inverter. Figure (a), for $t < 0$, the NMOS transistor is off and the PMOS transistor is on, forcing the output to the high state with $V_o = V_H = V_{DD}$. Figure (b), at $t = 0$, the input abruptly changes from 0 V to 5 V, and for $t = 0^+$, the NMOS transistor is on (V_{GS} = +5 V) and the PMOS transistor is off (V_{SG} = 0 V), and the capacitor voltage begins to fall as C is discharged through the NMOS transistor [3].